REMARKS

By this response, Applicants re-elect Species I, and reinstate the original claims 1-3, and 8-13, all readable on the elected species, as amended claims 21-29. Additionally, Applicants amend claims 21 and 24 to fully respond to the Office Action of , and request examination on the merits.

Original claims 4-7 and 14-20 are hereby withdrawn from consideration. Upon allowance of a generic claim, Applicants request rejoinder of all non-elected claims.

Title Objection

In the Office Actions of May 14, 2004, the title of the invention was objected to as not being descriptive. The title has been amended to read

SHIFT REGISTER ADOPTING A DATA CONVERSION CONTROL SYSTEM AND DRIVING CIRCUIT OF A LCD USING THE SAME

For these reasons, Applicants respectfully request withdrawal of the objection to the title.

Drawing Objection

In the Office Action of May 14, 2004, the drawings were objected to for being unclear at how the delay timing works in the entire m-row by n-column matrix. Applicants respectfully submit that for an m x n matrix, the memory devices in the same columns are subjected to the same delay, as described in the specification at page 6, lines 14-23 with reference to FIGs. 2 and 3. As recited at page 8, lines 3-5 of the specification, the configurations shown in FIGs. 2 and 3 can also be applied to the m x n matrix illustratively shown in FIG. 4. Although the delay units

shown in FIG. 2 do not appear in FIG. 4, it is clear from the description of FIG. 4, and the specification as a whole, that the illustrative embodiment illustrated in FIG. 4 may include such delay units. Thus, it is respectfully submitted that the original drawings sufficiently describe the delay timing function of the invention in an m row x n column matrix.

The same office action states that Figures 2 and 3 seem to demonstrate the propagation of data in the direction of columns, which is in conflict with the claim limitation of propagating in the direction of rows. Applicants respectfully submit that Figures 2 and 3 demonstrate the propagation of data in the direction of rows (e.g. from row to row) within a column, and thus, are consistent with the claim limitation. The terms "row" and "column" are clearly and distinctly defined in the specification, page 8, lines 11-20.

For these reasons, Applicant's respectfully request withdrawal of the drawing objection.

Specification Objection

In the Office Action of May 14, 2004, pages 6 and 7 of the specification were objected to as not clearly describing how the delay timing arrangement will be applied to an m x n matrix. As discussed above, Applicants respectfully submit that for an m row x n column matrix, the memory devices in the same rows are subjected to the same delay. Additionally, the paragraph beginning at page 8, line 6 was amended to read as follows:

> The above-described configuration of a shift register employing delay units, illustrated and explained with reference to FIGS. 2 and 3, can be also applied to a m row x n column matrix configuration. Specifically, the column of D flip flops M0, M1, M2, M3, shown in FIG. 2 correspond, respectively, to the column of D flip flops M00, M01, M02, M03, shown in FIG. 4. Though not shown in FIG. 4, delay units similar to the delay units 32, 34, 36 shown in FIG. 2 may be connected to the D flip flops M00, M01, M02, M03,

> respectively, in a manner similar to that illustrated in, and described in reference to, FIGs. 2 and 3.

For these reasons, Applicants respectfully request withdrawal of the objection to the specification.

Rejections under 35 U.S.C. § 112, second paragraph

Claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner stated it was unclear what the term "the result" in line 9 refers to, as there was insufficient antecedent basis for this term. The Examiner further stated that claim 1 was written in a way that made it difficult to read and understand.

In response, Applicants have amended Claim 1 (now claim 21) to incorporate at least a portion of the Examiner's suggested changes to make the claim more readable.

As amended, claim 21 recites, in part:

> ... a clock signal delay unit for gradually delaying a clock signal applied to said memory devices starting from an (m)th row (n)th column memory device that outputs data, progressing toward a first row of the memory devices where data is inputted;
>
> a data delay unit for delaying the data for a delay time of a clock signal that is applied to an input side of the memory devices; ....

For these reasons, Applicants respectfully request withdrawal of the § 112 rejection.

Rejections Under 35 U.S.C. § 102

Original claims 1-3 (now 21-23) stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U. S. Patent No. 3,708,690 issued to Paivinen ("Paivinen"). Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites:

> A shift register, comprising:
> memory devices formed in a shape of an m row x n column matrix and shifting data synchronized with a clock signal;
> a clock signal delay unit for gradually delaying a clock signal applied to said memory devices starting from an (m)th row (n)th column memory device that outputs data, progressing toward a first row of the memory devices where data is inputted;
> a data delay unit for delaying the data for a delay time of a clock signal that is applied to an input side of the memory devices; and
> a comparing unit to compare data inputted to the first row of memory devices with data outputted from the first row of memory devices, an output from the comparing unit to sequentially delay an operation of each of the memory devices to minimize data conversion and to prevent an instantaneous supply of electric power to multiple memory devices in each m row.

Paivinen does not disclose the comparing unit as recited. Instead, Paivinen teaches the simultaneous advancement of data from storage circuits 182, 184, 186, and 188 to the first stages 20A, 154A, 156A, and 158A. At the same time, a shift pulse is applied to the phase shift terminals of storage circuits 200, 202, 204, 206, and 208, to cause "...the data stored in the last register stages 20E, 154E, 156E, 158E, and 160E to advance to these storage circuits..." (Col. 12, lines 24-41). Thereafter, the data stored in the storage circuits 200, 202, 204, 206, and 208 is "sequentially advanced to the output terminal 198...." (Col. 12, lines 42-44). As noted in the Applicant's specification, page 10, lines 5-12, such simultaneous advancement of data through

the matrix requires a significant amount of instantaneous power supply, which generates harmful electromagnetic interference (EMI). As described at page 10, lines 13-20 of Applicant's specification, such teachings are contrary to the claimed invention, which recites a comparing unit to minimize simultaneous advancement of data (e.g. data conversion) through the m row x n column matrix.

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 102(b) rejection of claims1-3. Since none of the other prior art of record discloses or suggests all the features of the claimed invention, Applicants respectfully submit that independent claim 1, and all the claims that depend therefrom are allowable.

Rejections Under 35 U.S.C. § 103

Claims 8-13 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U. S. Patent No. 3,708,690 issued to Paivinen ("Paivinen") in view of U. S. Patent No. 5,245,326 issued to Zalph ("Zalph"). Applicants respectfully traverse this rejection for at least the following reasons.

Three criteria must be met to establish a prima facie case of obviousness. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not be based on applicant's disclosure, which is impermissible hindsight.

Independent claims 8 (now Reinstated claim 24), recites in part:

> ... a comparing unit to compare data inputted to the first row of memory devices with data outputted from the first row of memory devices, an output from the comparing unit to sequentially delay an operation of each of the memory devices to minimize data conversion and to prevent an instantaneous supply of electric power to multiple memory devices in each m row.

These features are not suggested or shown, singularly or in combination, by either Paivinen or Zalph. As aptly noted by the Examiner, Paivinen does not teach "...incorporating the register into LCD displays." Zalph does not compensate for Paivinen's omissions and shortcomings. In fact, Zalph teaches away from using such features as recited in the claimed invention.

Specifically, Zalph generically discloses shift registers 86 that operate in the conventional manner. (Col. 3, lines 23-34). In contrast, Applicant's specification and drawings show a storage register operated in a non-conventional manner using a comparing unit.

There is no motivation to combine the Paivinen and Zalph references. The lack of motivation arise from the fact that Paivinen is solving different problems than those addressed by Zalph. For example, Paivinen does not contemplate the use of a shift register in an LCD. Zalph contemplates test and calibration apparatus for LCD displays and generically references shift registers 86 in passing, without describing their structure or operation in detail. Thus, a person skilled in the art attempting to solve the problems addressed by the present invention, after viewing Zalph's teachings away, would not be motivated to look to solutions to the different problems addressed by Paivinen. Clearly, neither Paivinen nor Zalph, alone or in combination, teach the elements recited in independent claim 8, but rather teach in opposite directions altogether.

If anything, the combination of references, even though not teaching the presently claimed invention, would be impermissible hindsight reasoning. The only way one of ordinary skill in the art would look at Paivinen to use a shift register in a LCD view of the Zalph reference, would be to first read and understand the present invention. Only after reading and understanding the present invention, would one of ordinary skill in the art be provided with motivation to combine these references. And, this is respectfully submitted as impermissible hindsight, which in any event, still would not result in the claimed invention.

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of independent claim 8 (now Reinstated claim 24), and all claims that depend therefrom.

Added Claims

Claims 21-29 have been added. These claims correspond to and reinstate previously cancelled claims 1-3 and 8-13.

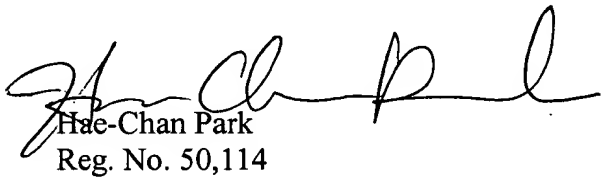
CONCLUSION

Applicants believe that a full and complete response has been made to the pending Office Action and respectfully submits that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicants respectfully submit that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicants' undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,



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